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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/808,049	03/24/2004	Timothy Henson	IR-2252 (2-3	4206

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EXAMINER	
LE, DUNG ANH	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 12/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/808,049	HENSON ET AL.	
	Examiner	Art Unit	
	DUNG A LE	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-17 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-17 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 24 March 2004 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DLe

DETAILED ACTION

Oath/Declaration

The oath/declaration filed on 3/24/2004 is acceptable.

Specification

The specification is objected to for the following reason:

The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: Claim 1, line 3, "a free surface of said semiconductor substrate"; line 16, "conductive region" ; line 18, "a first electrical contact"; line 19, "a second electrical contact" and line 18, "a free surface of said substrate".

The specification has been checked to the extent necessary to determine the presence of all possible minor errors. However, the applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 3-6, 8- 13and 17 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Background of Invention in view of Frisina (6586798).

Background of Invention discloses a process for manufacturing a power device comprising:

providing a semiconductor substrate 20 ;

growing epitaxially a first semiconductor layer 18 of a first conductivity over a free surface of said semiconductor substrate 20;

forming a mask over a free surface of said first semiconductor layer, said mask including a plurality of windows exposing portions of said semiconductor layer [0014] of Publication, and being capable of blocking implants; performing a series of implants through said implant windows to form a plurality of vertically

adjacent regions of a second conductivity in said first semiconductor layer below said implant windows; and

applying a diffusion drive to link said regions of said second conductivity to form vertically oriented regions of said second conductivity in said first semiconductor layer [0015];

forming a channel region 12 (refer to figs. 1 and 2) of said second conductivity above said first semiconductor layer; forming a plurality of MOS-gated structures 14-16 through said channel region; forming conductive regions 26 of said first conductivity adjacent each MOS-gated structure;

forming a first electrical contact 22 on a free surface of said substrate; and forming a second electrical contact 24 in electrical contact with at least said conductive regions of said first conductivity;

Background of Invention does not disclose vertically oriented regions of said second conductivity are in substantial charge balance with said first semiconductor layer.

Frisina teaches vertically oriented regions of said second conductivity are in substantial charge balance with said first semiconductor layer (col 6, lines 12-15).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form vertically oriented regions of said second conductivity are in substantial charge balance with said first semiconductor layer in Background of Invention 's method, in order to improve the functional units are able to withstand the high voltage in which power device operates.

Regarding claim 3, wherein said vertically oriented regions 28 of said second conductivity are less than 5 microns wide (Table 1) in Background of Invention.

Regarding claim 4, wherein said channel region 12 is formed by growing an epitaxial semiconductor layer of said second conductivity (fig. 1).

Regarding claim 5, wherein said channel region 12 is formed by implanting dopants (P-) of said second conductivity into said epitaxial semiconductor layer (fig. 1) Background of Invention .

Regarding claim 6, further comprising: growing epitaxially a second semiconductor layer 18" of said first conductivity N over said first semiconductor layer 18 of said first conductivity refer to Background of Invention;

forming a second mask [0015]over a free surface of said second semiconductor layer, said second mask including a plurality of windows exposing portions of said second semiconductor layer, and being capable of blocking

implants; and performing a series of implants through said implant windows in said second mask to form a plurality of vertically adjacent regions of said second conductivity in said second semiconductor layer below said implant windows and above said vertically oriented regions 28 of said second conductivity in said first semiconductor layer.

Regarding claim 8, wherein said vertically oriented regions of said second conductivity are less than 5 microns wide.

Regarding claim 9, wherein said channel region 12 is formed by growing an epitaxial semiconductor layer of said second conductivity (P-) in fig. 1.

Regarding claim 10, wherein said channel region 12 is formed by implanting dopants of said second conductivity (P-) into said second semiconductor layer (fig. Background of Invention).

Regarding claim 11, wherein said conductive regions 10 of said first conductivity are source regions.

Regarding claim 12, wherein said first electrical contact is a drain contact 22 , and said second electrical contact is a source contact 24 (fig. 1 Background of Invention).

Regarding claim 13, wherein said semiconductor substrate is of first conductivity (N+).

Regarding claim 17, wherein said growing of an epitaxial semiconductor layer, said forming a mask, said performing a series of implants and said applying a diffusion drive are repeated more than two times (fig. 2) in Background of Invention.

Claims 2, 7 and 14-16 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Background of Invention in view of Frisina (6586798) and further in view of the following remark.

Regarding claim 2, Background of Invention in view of Frisina teach the claimed invention as applied to claim 1, except for the implant windows are 0.25 to 2.0 microns wide.

It would have been obvious to one having ordinary skill in the art at the time of the invention was made to form the implant windows are 0.25 to 2.0 microns wide, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art.

Regarding claim 7, Background of Invention in view of Frisina teach the claimed invention as applied to claims 1 and 6, except for the implant windows are 0.25 to 2.0 microns wide. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the implant windows are 0.25 to 2.0 microns wide, since it has been held that where the general conditions of a

claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art.

Regarding claim 14-16, Background of Invention in view of Frisina teach the claimed invention as applied to claim 1, except for the mask is comprised of an oxide, wherein said mask is comprised of photoresist and wherein said mask is comprised of a nitride. It would have been obvious to one having ordinary skill in the art at the time the invention was made to form the mask by utilizing the above mentioned material, because they are commonly used to prevent undesirable reactions in the implanting region, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use.

When responding to the office action, Applicants' are advice to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist the examiner to locate the appropriate paragraphs.

A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to become abandoned (see M.P.E.P 710.02(b)).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dung A. Le whose telephone number is (571) 272-1784. The examiner can normally be reached on Monday-Tuesday and Thursday 6:00am- 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571) 272-1787. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9306 for regular communications and (703) 872-9306 for After Final communications.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DUNG A. LE DL
Primary Examiner
Art Unit 2818